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09/144,579	08/31/1998	DAH WEN TSANG	1138-71	4972

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EXAMINER
LOKE, STEVEN HO YIN

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2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/144,579	Applicant(s) TSANG ET AL.
	Examiner Steven Loke	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *43-66,98-103,106 and 107* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *43-66,98-103,106 and 107* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The drawings are objected to because the newly submitted fig. 6B of the present application does not match with fig. 19 of U.S. patent no. 4,895,810. Fig. 19 of U.S. Patent no. 4,895,810 shows the layer [75] is formed below region [24]. However, newly submitted fig. 6B shows layer [275] is at the same level as region [224]. The newly submitted fig. 6C of the present application does not match with fig. 16B of U.S. patent no. 5,262,336. Figs. 16A and 16B of U.S. patent no. 5,262,336 show a portion of layer [72] is also formed under a part of each of the sidewalls [62]. However, newly submitted fig. 6C shows layer [272] is not formed under the sidewalls [262]. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. Claims 45, 60-66 and 99-102 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification inherently discloses an upper metal layer over the insulating layer and contacting the gate conductor through a via in the insulating layer (claim 44). However, the specification never discloses a portion of the upper metal layer as claimed in claim 44 also contacts the source conductor as claimed in claim 45. The claimed invention would create a short circuit between the source electrode and the gate electrode.

Newly submitted fig. 6B shows a planar gate type MOSFET having a gate electrode comprising polysilicon [232], a tungsten layer [276] and a plated metal layer or an aluminum layer on the tungsten layer. However, the specification never discloses the gate electrode of fig. 6B can also applied to the gate electrode of a trench-type gate MOSFET. Therefore, the specification never discloses the gate metal layer of a trench-type gate electrode comprises aluminum as claimed in claims 60, 64, 65, 66, 99 and 102. The specification only discloses the gate metal layer comprises a refractory metal silicide (page 11, line 27 to page 12, line 1).

The specification also never discloses the gate electrode of a trench-type gate electrode comprises a plateable metal as claimed in claims 61, 63 and 100.

The specification also never discloses the gate electrode of a trench-type gate electrode comprises a refractory metal silicide beneath the gate metal layer as claimed in claims 62 and 99.

The specification never discloses the insulative layer is deposited at temperature less than 430 degree C as claimed in claim 101.

3. Claims 50, 98 and 101 are objected to because of the following informalities: Claim 98, line 14, the phrase "doped a polysilicon layer" is unclear whether it is being referred to "a doped polysilicon layer". Claim 50, lines 3-4, the phrase "the vertically-oriented layers" has no antecedent basis. Claim 101, line 1, the phrase "the insulative layer" has no antecedent basis. Appropriate correction is required.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 43, 47, 48, 50, 51, 53, 57, 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto.

In regards to claim 43, 50, 51, 53, 57, Sakamoto discloses a transistor in fig. 4(d). It comprises: a gate trench formed on a drain substrate [1,3]; p-type body region [11], vertical channel regions and source regions [12] formed between the trenches; vertically-insulative layers [4] formed on the gate insulation layers [7] and the source regions [12]; the laterally-extending insulative layer [9] formed on the gate electrode [8]; a source electrode [15] formed on the regions [11, 12, 9] and opposite to the gate electrode [8].

Sakamoto differs from the claimed invention by not having a gate metal layer coextending over a doped polysilicon of a gate conductor.

Fig. 2(d) of Sakamoto shows a metal silicide (tungsten silicide) layer formed on a doped polysilicon gate conductor [8] in a vertical MOSFET.

Since both figs. 4(d) and 2(d) of Sakamoto teach a polysilicon gate electrode in a vertical MOSFET, it would have been obvious to have the metal silicide layer and doped polysilicon gate electrode of fig. 2(d) of Sakamoto in fig. 4(d) of Sakamoto because they reduce the resistance of the gate electrode.

Sakamoto further differs from the claimed invention by not showing the gate insulating layer is made of oxide. It would have been obvious to have the gate insulating layer made of oxide, since it has been held to be within the general skill of a

worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

In regards to claim 47, fig. 4(d) of Sakamoto differs from the claimed invention by not showing the first vertical layer portion has a lateral thickness less than a vertical height thereof.

Fig. 3 of Sakamoto shows the first vertical layer portion [11] has a lateral thickness less than a vertical height thereof.

Since both figs. 4(d) and 3 of Sakamoto teach a source electrode formed in a trench in a vertical MOSFET, it would have been obvious to have the p-type base region of fig. 3 of Sakamoto in fig. 4(d) of Sakamoto because it reduces the resistance of the base region.

In regards to claim 48, the combined device of Sakamoto differs from the claimed invention by not showing the first vertical layer portion has a lateral thickness less than 1 micron. It would have been obvious for the first vertical layer portion has a lateral thickness less than 1 micron because it depends on the size of the transistor cell and the packing density of the transistor cells.

In regards to claim 58, fig. 4(d) of Sakamoto differs from the claimed invention by not showing a base region made of p-type layer.

Fig. 7 of Sakamoto shows a p-type layer [1'] formed under the n-type layer [2, 3].

Since figs. 4(d) and 7 of Sakamoto show a vertical transistor, it would have been obvious to have the p-type layer of fig. 7 of Sakamoto in fig. 4(d) of Sakamoto because it reduces the on-resistance of an insulated gate bipolar transistor.

6. Claims 44, 46, 55, 56, 98, 103, 106 and 107 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined device of Sakamoto as set forth in paragraph no. 5 in view of Bulucea et al.

In regards to claims 44, 98, 106, Sakamoto differs from the claimed invention by not showing an insulating layer over the gate conductor and an upper metal layer over the insulating layer and contacting the gate conductor through a via in the insulating layer.

Bulucea et al. shows an insulating layer [41] over the gate conductor [36a, 36b] and an upper metal layer [43a] over the insulating layer and contacting the gate conductor through a via in the insulating layer in figs. 21-31B.

Since both Sakamoto and Bulucea et al. teach a vertical MOSFET with a trench-type gate electrode, it would have been obvious to have the gate contact structure of Bulucea et al. in Sakamoto because it provides external connection between the MOSFET and the external circuit.

In regards to claim 46, the combined device shows the insulating layer [9 of Sakamoto] over the gate conductor [8] and the source electrode [15] over the insulating layer and contacting the vertically-extending source conductor through a via in the insulating layer [9]. Bulucea et al. further show the source electrode [43b] can be made of metal.

In regards to claim 52, the combined device shows the source electrode [15 of Sakamoto] extending over the insulative layer [9] and the vertically-oriented sidewall spacers [4] and contacting the vertically-extending source conductor. Bulucea et al. further show the source electrode [43b] can be made of metal.

In regards to claims 55, 107, the combined device (figs. 2b, 21-31B of Bulucea et al. and Sakamoto) shows the trench-type gate structure enclosing a plurality of cells that comprises the source conductor and the source and channel regions.

In regards to claim 56, the combined device (figs. 2b, 21-31B of Bulucea et al. and Sakamoto) shows the insulated trench-type gate formed a gate structure configured as a finger. The combined device further comprises a plurality of said fingers, and the source conductor intermediate the fingers of the plurality of gate fingers to define an interdigitated source-gate structure.

In regards to claim 103, the combined device differs from the claimed invention by not showing the metallization over the insulating layer comprises aluminum. It would have been obvious for the metallization over the insulating layer comprises aluminum, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

7. Claims 49 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Davies.

Sakamoto differs from the claimed invention by not showing a p+ type body region.

Davies shows a p+ type body region [21] formed in a p-type base region [17] in a vertical MOSFET in fig. 1.

Since both Sakamoto and Davies teach a vertical MOSFET, it would have been obvious to have the p+ type body region of Davies in Sakamoto because it prevents

parasitic bipolar transistor turn on and it extends the safe operating area of the transistor.

8. Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Blanchard.

In regards to claim 59, Sakamoto further differs from the claimed invention by not showing a trench gate oxide with two different thickness.

Blanchard shows the gate oxide layer [32] having a thick oxide layer at the bottom of the gate trench and a thin oxide layer at the upper portion of the gate trench in fig. 3.

Since both Sakamoto and Blanchard teach a vertical MOSFET with a trench gate, it would have been obvious to have the gate oxide layer of Blanchard in Sakamoto because it increases the breakdown voltage of the device.

9. Applicant's arguments filed 11/29/02 have been fully considered but they are not persuasive.

It is urged, in pages 11-12 and 18-19 of the remarks, that silicide is not considered as a metal layer. However, the first full paragraph of page 376 of Sze shows silicides are important metallization materials for semiconductor device. Therefore, the silicide layer of applicants' specification is considered as a metal layer.

It is urged, in page 13 of the remarks, that the process to form the oxide layer [10] and impurity regions [11, 12] would employ temperatures incompatible with provision of a metal layer coextensively over the polysilicon for a gate conductor in a trench as set forth in claim 43. However, the manufacturing processes of both of the devices (fig. 2(d) and fig. 4(d)) of Sakamoto involve oxidation of the polysilicon gate electrode to form

a top gate oxide and ion-implantation to form the source and body regions. Since the silicide layer is formed before the top gate oxide in the device of fig. 2(d) of Sakamoto, it is believed that the device of fig. 4(d) is also able to form the top gate oxide after the silicide is formed on the polysilicon gate electrode. The combined device of Sakamoto shows a metal layer (tungsten silicide) over doped polysilicon of a gate conductor to a field effect power MOS device with a vertically-oriented channel. Sakamoto meets the limitation of the claimed invention.

It is urged, in pages 14-15 of the remarks, that Bulucea never discloses a metal layer co-extensive over polysilicon for a gate conductor within a trench of a field effect power MOS device. However, the combined device of Sakamoto shows a metal layer (tungsten silicide) over doped polysilicon of a gate conductor to a field effect power MOS device. Therefore, the combined device of Sakamoto and Bulucea also shows a metal layer (tungsten silicide) over doped polysilicon of a gate conductor to a field effect power MOS device. In addition, the combined device also teaches an upper metal layer connected to the gate conductor as claimed in claim 44.

It is urged, in page 17 of the remarks, that an artisan in the field of vertically-oriented channel regions may not look at the teachings of Davies. However, both Sakamoto and Davies disclose a vertical MOSFET having a body region under the channel region. Therefore, it is reasonable to have the p+ type body region of Davies in Sakamoto.

It is urged, in page 18 of the remarks, that the metal layer would prevent the oxidation of an upper portion of silicon of the gate to form a flat surface as taught by Blanchard. However, fig. 2(d) of Sakamoto shows the polysilicon gate can be oxidized

after a silicide layer formed on the gate electrode. Therefore, the metal silicide of Sakamoto would not prevent the oxidation of an upper portion of silicon of the gate to form a flat surface as taught by Blanchard.

It is urged, in pages 19-20 of the remarks, that claims 60-65 are supported in the specification. As mentioned in the rejection, newly submitted fig. 6B shows a planar gate type MOSFET having a gate electrode comprising polysilicon [232], a tungsten layer [276] and a plated metal layer or an aluminum layer on the tungsten layer. The original specification never discloses the gate electrode of a planar gate type MOSFET of fig. 6B can be applied to the gate electrode of a trench-type gate MOSFET.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

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March 9, 2003

Primary Examiner
Steven Loke